

New Dynamic FET Logic and Serial Memory Circuits for VLSI GaAs Technology

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Abstract- The complexity of GaAs FET VLSI circuits is limited by the maximum power dissipation while the uniformity of the device parameters determines the functional yield. In this work, novel digital GaAs FET circuits are presented that eliminate the dc power dissipation, reduce the area to 50% of that of the conventional static circuits and its larger tolerance to device parameters variations, results in higher functional yield.

1 Introduction

GaAs technology is used in the fabrication of ultra fast digital integrated circuits. The availability of such circuits is critical for many applications such as Gigabit communication systems and super fast computers [1]. The GaAs FET is fundamentally different from both the MOSFET and the bipolar transistor. Figure 1 highlights these differences.

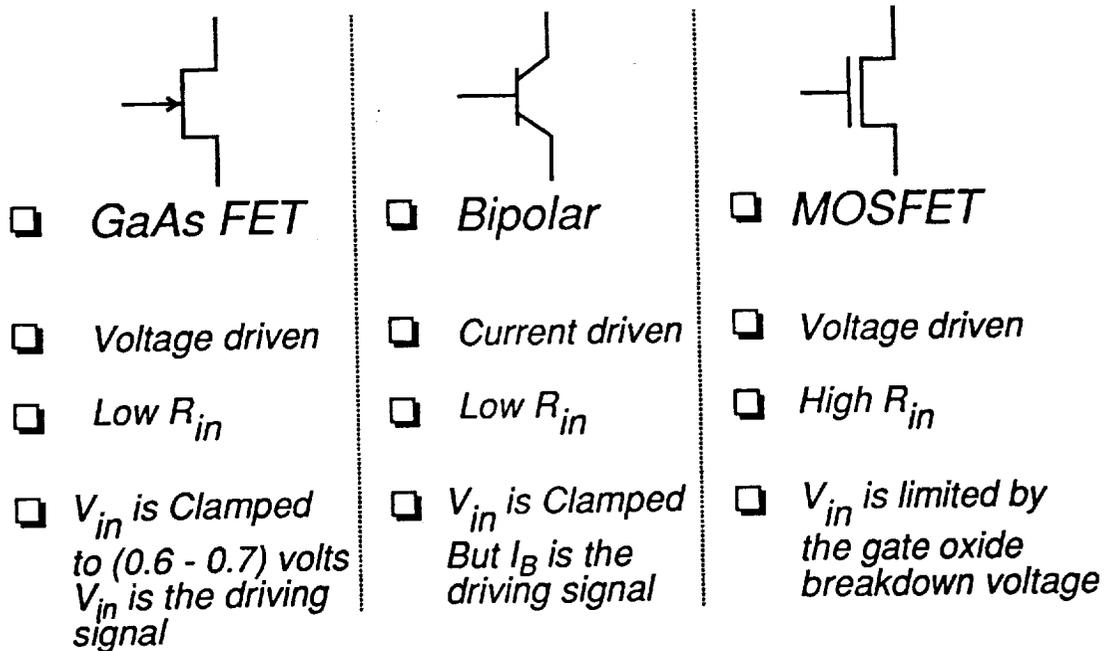


Figure 1: Fundamental differences between devices

Because of these differences, the bipolar and MOS logic families and circuit techniques

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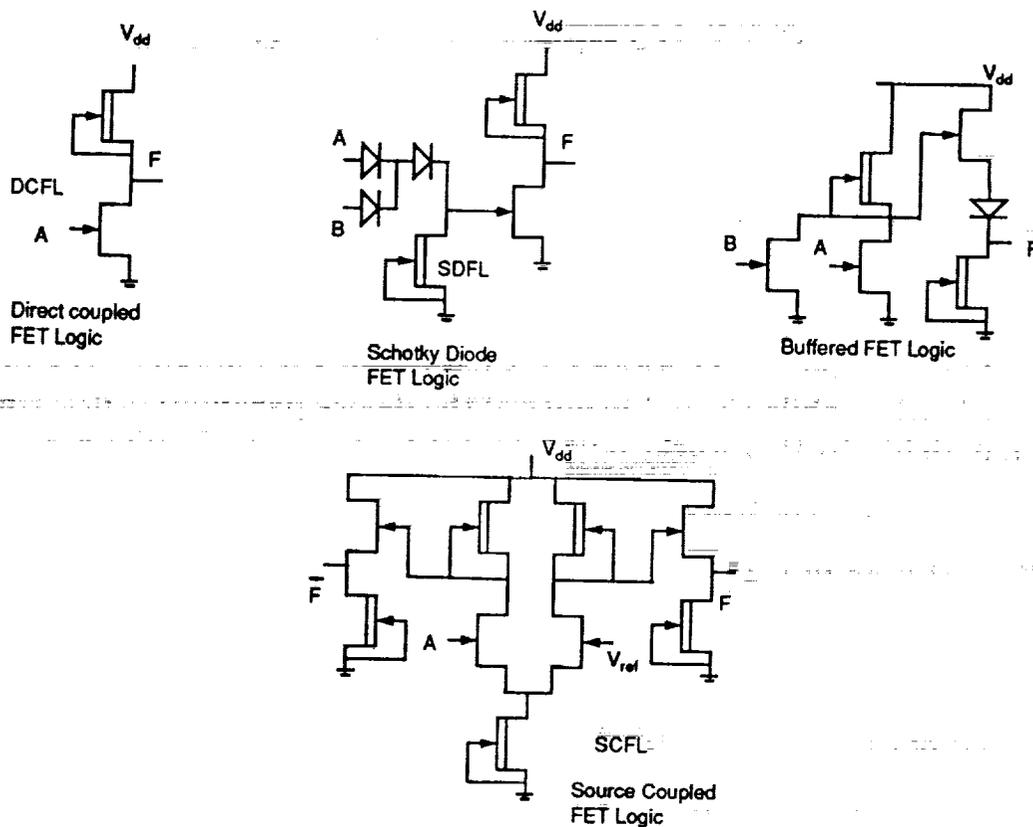


Figure 2: Static GaAs FET logic families

Because of these differences, the bipolar and MOS logic families and circuit techniques will be less successful if applied directly without modification to the GaAs technology. Figure 2 shows the most commonly used static GaAs FET logic families [1].

In any of the two logic state, all these circuits will dissipate dc power. This dc component accounts for 90% of the total power [2]. The power dissipation limits the maximum number of gates to 15,000 assuming a maximum allowable chip power of 5 watts [2]. On the other hand, the ratio of the threshold voltage variation to the noise margin is critical for determining the IC electrical yield. It is shown that if the threshold voltage variance is changed from 90 mv to 150 mv, the circuit size should be reduced from 10,000 to 100 gates to maintain 50% yield [2]. This illustrates that the threshold voltage must be tightly controlled for acceptable yield. In this paper, a novel circuit technique [3]-[6] is applied to GaAs HFET technology to overcome these two main limitations. The new memory and logic circuits do not dissipate any dc power, are less sensitive to threshold voltage variation and have very small size.

2 The D-Type Flip Flop

An intermediate stage of a dynamic shift register is shown on Figure 3 a. The D-type flip flop uses depletion type transistors with threshold voltage of (-0.7 volts). Figure 3 b shows the clock and input waveforms and the logic levels.

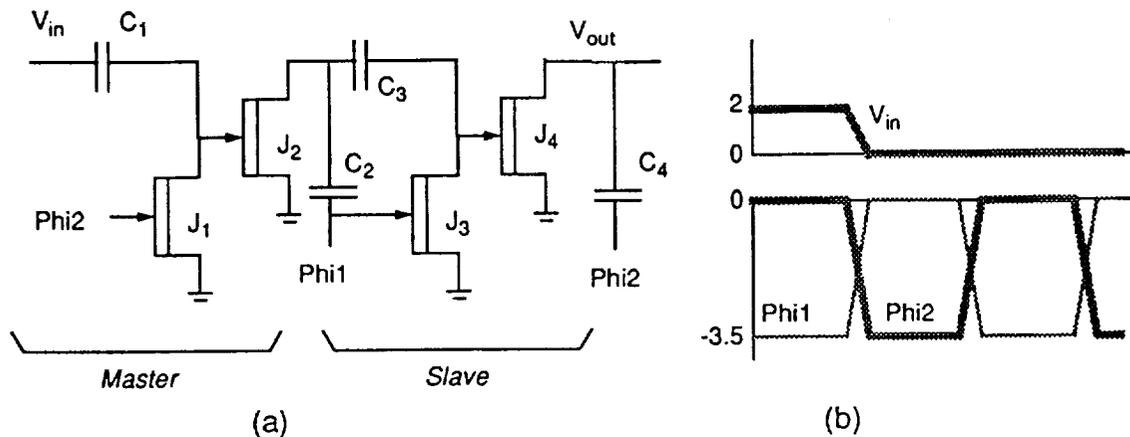


Figure 3: M/S dynamic D-type Flip Flop (*intermediate stage*)

During t_1 , $\text{Phi}2 = 0$ volts. The master section is in the sample phase. The input data is stored on the capacitor C_1 . It is charged to 2 volts or discharged to 0 volts for V_{in} being logical 1 or 0 respectively. The capacitor C_2 is precharged to approximately 3.5 volts through J_2 ($\text{Phi}1 = -3.5$ volts). The slave section is in the evaluation phase. Transistor J_3 is cut off and the drain voltage of J_2 , $V_{D2} = 0$ volts, thus providing a reference voltage for evaluating the stored data on C_3 . If C_3 is charged, J_4 is turned off and the precharged capacitor C_4 retains its voltage to represent logic 1. However, if C_3 is discharged, J_4 is turned on and C_4 is discharged to represent logic 0. During t_2 , the roles of the master and slave sections are interchanged. Figure 4 shows the output stage of the shift register.

The capacitor C_4 is replaced by a pull up device for interfacing with static logic (DCFL). The simulation results for the output stage are shown in Figure 5. The device model accounts for the second order effects and is accurately calibrated to a 1 μm HFET process. Figure 5(a) shows that V_{out} is delayed by one clock period with respect to V_{in} which verifies the operation of the D-Type flip flop at 2 GHz. Figure 5(b) shows the waveforms V_{D1} , V_{D2} and V_{D3} which correspond to the drain voltage of J_1 , J_2 and J_3 respectively.

Table 1 compares the dynamic and static (DCFL) implementations of the D-Type flip flop.

Each section of the DCFL (M/S) Flip Flop uses two inverters for the static memory cell, two depletion transistors (clocked transmission gates) and two DCFL super buffers, as shown in Figure 6, to properly buffer the memory cell from the direct and capacitive coupling caused by the clock signals driving the transmission gates. This DCFL implementation requires 24 transistors of both depletion and enhancement types. Table 1 shows

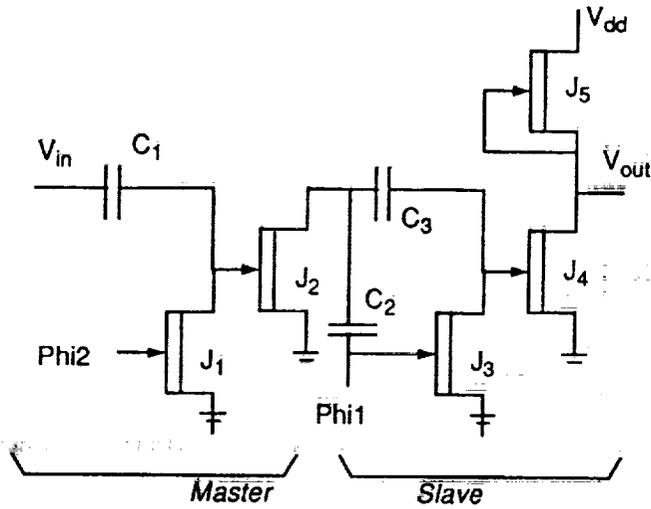
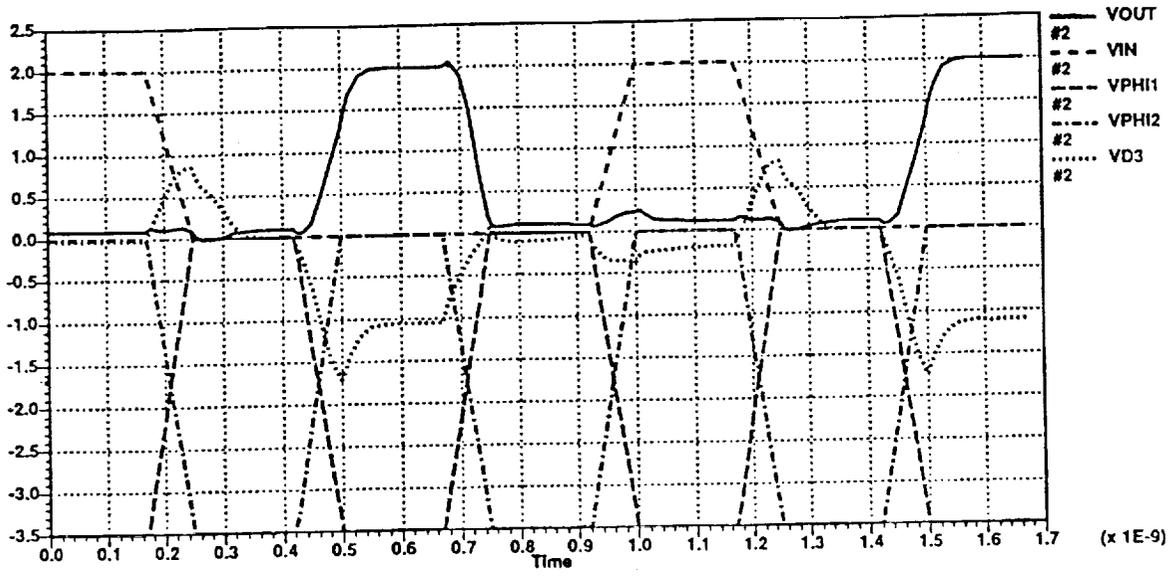


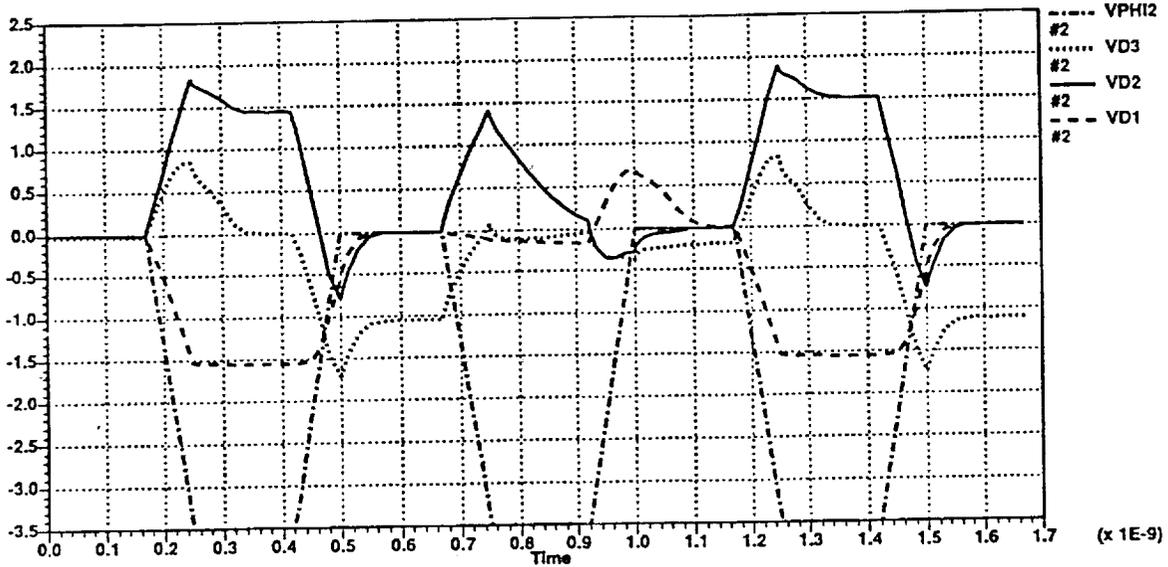
Figure 4: M/S dynamic D-type Flip Flop (Output stage)

	Dynamic FF	Static FF
Power	0.4 mw	4 mw
Number of devices	4 transistors 4 capacitors	24 trnsistors
Relative area	0.3	1
Noise margin (NM)	500 mv	200 mv

Table 1: Dynamic and static implementations of the D-Type flip flop



(a)



(b)

Figure 5: Voltage waveforms of the M/S D-Type Flip Flop

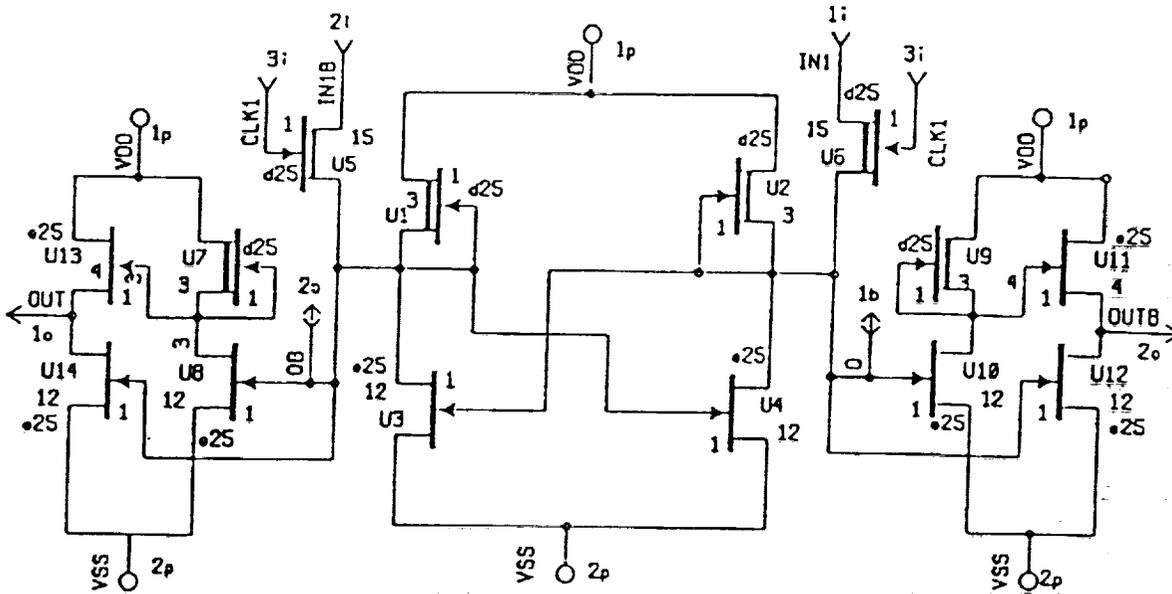


Figure 6: DCFL implementation of one section of the M/S D-Type Flip Flop

that the dynamic circuit has significant savings in both power dissipation and area. The larger functional yield can be measured by the ratio of the threshold voltage variation to the noise margin. Figure 5 shows that V_{D1} swings between -1.2 and 0 volts with a threshold voltage of -0.7 volts. This relatively large noise margin makes the circuit operation less sensitive to threshold voltage variations and results in a larger functional yield.

3 Logic circuits implementation

The basic dynamic circuit can also be used to implement the AND, OR, and complex logic functions. The operation of the basic circuit is similar to that of the dynamic flip flop. Figure 7 summarizes the operation.

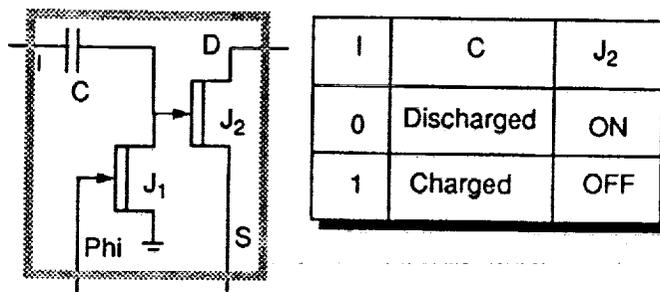


Figure 7: Basic dynamic logic circuit

A	B	C ₁	C ₂	J ₁	J ₂	F
1	1	charged	charged	OFF	OFF	1

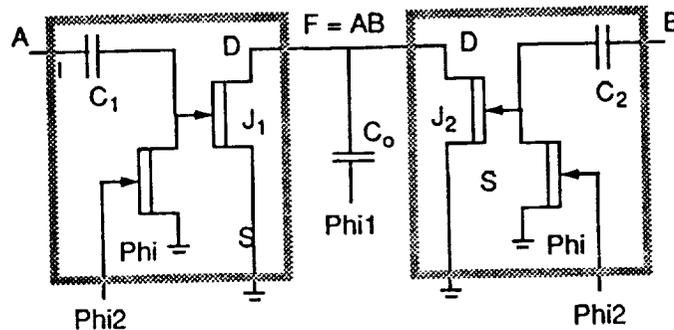


Figure 8: The dynamic AND function

When the input is logic 0, the capacitor C is discharged during the sampling phase and the transistor J_2 will turn on during the evaluation phase. Similarly, if the input is logical 1, the capacitor is charged during the sampling phase causing J_2 to turn off during the evaluation phase.

An AND function is realized by connecting two cells in parallel as shown in Figure 8. During the evaluation phase, the output will remain charged (representing logic 1) if both J_1 and J_2 are turned off. This corresponds to $A = B = 1$ during the sampling phase. Any other combination for the values of the inputs A and B will result in at least one of J_1 or J_2 being turned on and causing the output to correspond to logic 0.

The OR function is implemented by connecting cells in series as shown in Figure 9. During the evaluation phase, the output will be discharged only if both J_1 and J_2 are turned on. This corresponds to $A = B = 1$ during the sampling phase. If A or B is logic 1, at least one of the transistors J_1 or J_2 will be turned off during the evaluation phase. This causes the output to remain charged and correspond to logic 1.

Complex logic gates can be realized by parallel and series connections of the basic circuit as shown in Figure 10. In this example the output F will remain charged during the evaluation phase if either (C and D) are logic 1 during the sampling phase or (A and B) are logic 1. This ensures that there is no discharge path from the output to ground during the evaluation phase.

It is seen that these logic circuits do not dissipate any dc power. Also, since only one type (depletion) of transistors is used, the circuits are less sensitive to process and threshold voltage variations. It is noted that when the clocked depletion transistors are turned on, $V_{GS} = 0$ volts and the transistors do not draw any gate current. V_{GS} can be increased to about 0.4 volts, which will keep the gate current negligibly small while increasing the driving capability of the clocked transistors and the noise margin of the circuit. This will also enhance the operating speed.

A	B	C ₁	C ₂	J ₁	J ₂	F
0	0	discharged	discharged	ON	ON	0

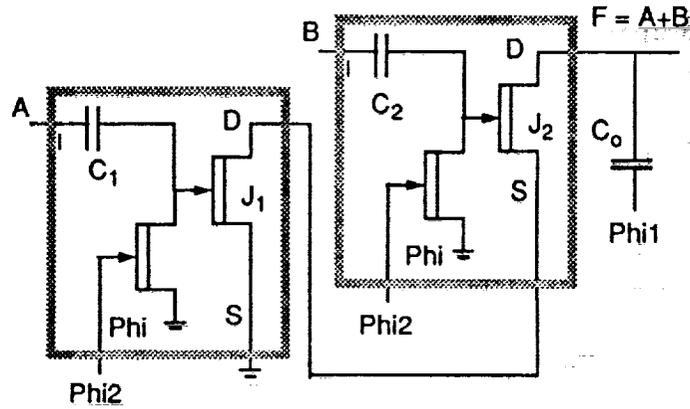


Figure 9: The dynamic OR function

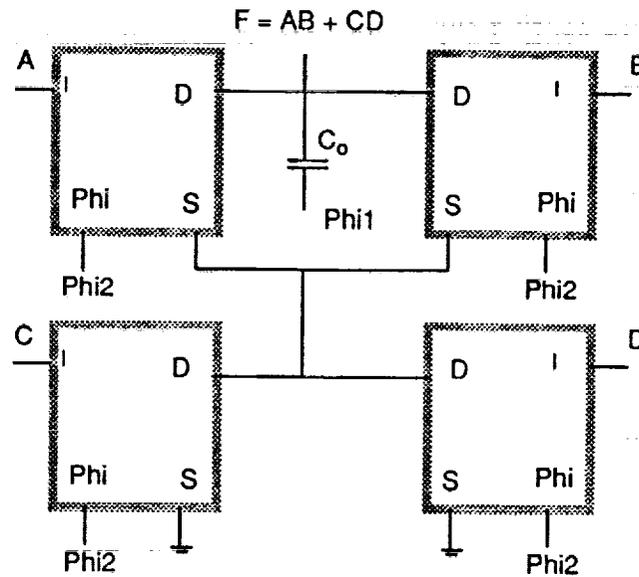


Figure 10: The dynamic Complex Logic gate

4 Conclusions

The new dynamic circuits eliminate the dc power and have large noise margin and small size. Compared to the static implementation using the DCFL, the use of the dynamic circuits results in (50-70)% reduction in the area. The noise margin and therefore the electrical functional yield is increased by a factor of 2.5 and the total power dissipation is reduced by 90% at a switching speed of 2 GHz. These significant improvements allow an order of magnitude higher level of integration with acceptable functional yield and power dissipation.

References

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